10 MHz Bandwidth, 640 MSPS Dual Continuous Time Sigma-Delta Modulator

Preliminary Technical Data

AD9267

FEATURES

SNR: 83 dB (85 dBFS) to 10 MHz input
SFDR: 87 dBc to 10 MHz input
Noise figure: 15 dB
Input impedance: 1 kΩ
Power: 415 mW
10 MHz real or 20 MHz complex bandwidth
1.8 V analog supply operation
On-chip PLL clock multiplier
On-chip voltage reference
Twos complement data format
640 MSPS, 4-bit LVDS data output
Serial control interface (SPI)

APPLICATIONS

Baseband quadrature receivers: CDMA2000, WCDMA, multicarrier GSM/EDGE, 802.16x, and LTE
Quadrature sampling instrumentation

GENERAL DESCRIPTION

The AD9267 is a dual continuous time sigma-delta (Σ-Δ) modulator with 86 dB of dynamic range over 10 MHz real or 20 MHz complex bandwidth. The combination of high dynamic range, wide bandwidth, and characteristics unique to the continuous time Σ-Δ modulator architecture make the AD9267 an ideal solution for wireless communication systems.

The AD9267 has a resistive input impedance that significantly relaxes the requirements of the driver amplifier. In addition, a 32× oversampled fifth-order continuous time loop filter attenuates out-of-band signals and aliases, reducing the need for external filters at the input. The low noise figure of 15 dB relaxes the linearity requirements of the front-end signal chain components and the high dynamic range reduces the need for an automatic gain control (AGC) loop.

A differential input clock controls all internal conversion cycles. An external clock input or the integrated integer-N PLL provides the 640 MHz internal clock needed for the oversampled continuous time Σ-Δ modulator. The digital output data is presented as 4-bit, LVDS at 640 MSPS in twos complement format. A data clock output (DCO) is provided to ensure proper latch timing with receiving logic. Additional digital signal processing may be required on the 4-bit modulator output to remove the out-of-band noise and to reduce the sample rate.

FUNCTIONAL BLOCK DIAGRAM

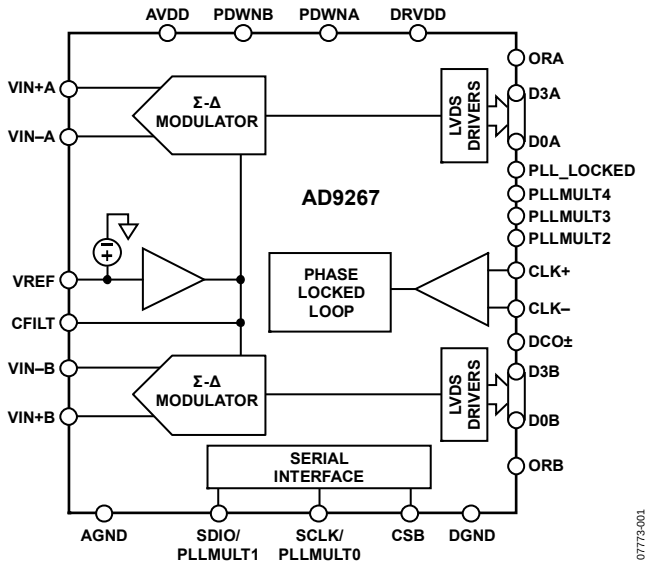

Figure 1.

The AD9267 operates on a 1.8 V power supply, consuming 415 mW. The AD9267 is available in a 64-lead LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Continuous time Σ-Δ architecture efficiently achieves high dynamic range and wide bandwidth.
2. Passive input structure reduces or eliminates the requirements for a driver amplifier.
3. An oversampling ratio of 32× and high order loop filter provide excellent alias rejection reducing or eliminating the need for antialiasing filters.
4. Operates from a single 1.8 V power supply.
5. A standard serial port interface (SPI) supports various product features and functions.
6. Features a low pin count, high speed LVDS interface with data output clock.

Rev. PrA

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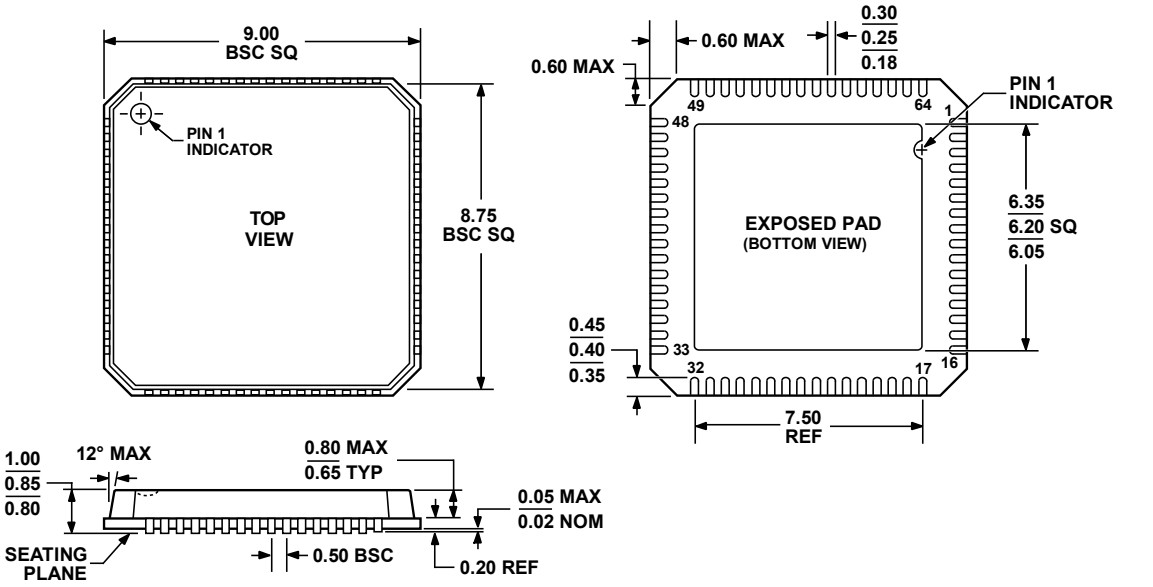
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 2. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9267BCPZ[1, 2]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	TBD
AD9267EBZ[1]		Evaluation Board	

[1] Z = RoHs Compliant Part.
[2] It is required that the exposed paddle be soldered to the AGND plane to achieve the best electrical and thermal performance.

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